DEGREE CURRICULUM

COMPUTER ORGANIZATION II

Coordination: SAIZ VELA, ALBERT

Academic year 2023-24

COMPUTER ORGANIZATION II 2023-24

Subject's general information

Subject name	COMPUTER ORGANIZATION II
Code	105003
Semester	2nd Q(SEMESTER) CONTINUED EVALUATION
Typology	<table><tr><th>Degree</th><th>Course</th><th>Character</th><th>Modality</th></tr><tr><td>Bachelor's Degree in Computer Engineering</td><td>1</td><td>COMMON/CORE</td><td>Attendance-based</td></tr></table>
Course number of credits (ECTS)	6
Type of activity, credits, and groups	<table><tr><th>Activity type</th><th>PRALAB</th><th>TEORIA</th></tr><tr><th>Number of credits</th><td>3</td><td>3</td></tr><tr><th>Number of groups</th><td>2</td><td>1</td></tr></table>
Coordination	SAIZ VELA, ALBERT
Department	COMPUTER ENGINEERING AND DIGITAL DESIGN
Teaching load distribution between lectures and independent student work	Globally, the subject has 60 hours of face-to-face classes and 90 hours of independent student work.
Important information on data processing	Consult this link for more information.
Language	Catalan
Distribution of credits	3 credits Theory --> 30 hours of face-to-face classes + 45 hours of autonomous work from the student side. 3 credits Pralab (Problems + Lab) --> 30 hours of face-to-face classes + 45 hours of autonomous work from the student side.

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Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
PUIGGROS FIGUERAS, DAVID	david.puiggros@udl.cat	3	
SAIZ VELA, ALBERT	albert.saiz@udl.cat	3	
TOMAS GLEYAL, MARC	marc.tomas@udl.cat	3	

Subject's extra information

To follow this subject properly some previous knowledge/skills on computer organization are recommended.
According to this, it must have taken the subject of Computer Organization I, which is scheduled in the first semester of the first course.
The skills acquired in this course are required to take the course of Computer Architecture of the second degree course.

Learning objectives

- Implement simple programs written in assembly language.
- Identify, differentiate and understand the operation of a computer, its components, as well as the basic
- structure of Von-Neumann.
- Know the phases of instruction execution.
- Be able to propose a basic structure for an instruction set.
- Identify the components of the control unit and their interaction.
- Be able to propose a basic structure for the main memory of a computer.
- Identify and understand the system input / output within the structure of a computer.
- Help other group members if necessary.
- Find and justify the best solution in a given time.

Competences

Degree-specific competences

GII-FB3: Capacity to understand and master the basic concepts of discreet mathematics, logical, algorithmic and computational complexity, and its application to solve engineering problems.

GII-FB4: Basic knowledge of the use and programming of computers, operating systems, databases and computer programs with applications in engineering.

GII-FB5: Knowledge of the structure, organisation, operation and interconnection of the computer systems, the basics of programming, and its application to solve engineering problems.

GII-CR17: Knowledge, design and efficient use of the types and data structure more suitable for solving a problem.

GII-CR19: Capacity to know, comprise and evaluate the structure and architecture of computers, as well as the basic components that conform them.

Degree-transversal competences

EPS1: Capacity to solve problems and prepare and defence arguments inside the area of studies.

EPS5: Capacity of abstraction and of critical, logical and mathematical thinking.

EPS9: Capacity for unidisciplinary and multidisciplinary teamwork.

EPS12: To be motivated for the quality and steady improvement.

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Subject contents

1.- Introduction

1.1. Structure of a Von-Neumann Computer

1.2. Interconnection Structures.

1.3. Instruction Cycle

2.- Instruction set

2.1. Introduction.

2.2. Formats of Instruction.

2.3. Addressing modes

2.4. Types of operations.

2.5. Von Neumann Simulator.

3. Control Unit

3.1. Introduction and Functions

3.2. Control Signals.

3.2. Hardwired Control Unit.

4. Memory Unit

4.1. Global Concepts

4.2. Memory Hierarchy.

4.3. Random Access Memory

5. Input/Output System

5.1. General I/O system.

5.2. Addressing I/O.

5.3. Control / synchronization of I/O: Check State and Interruptions.

5.4. Access to I/O Data: Program-Driven and Direct Memory Access.

Methodology

Large Group: theory class (3 ECTS)
In this group, the theoretical contents of the subject, accompanied by illustrative examples, will be explained. As support material class, there are the slides of the subject, which can be downloaded from the CV Sakai.

Medium Group: Problems / Laboratory Classes (3 ECTS)
In this group, solving problems from the collection will be alternated along with performing practices of assembly programming. The material of the Laboratory will be posted on the CV Sakai of the subject. Thestudent must attend class practices with statements previously read.

Self study (distance learning)
The student should independently solve problems not done in class, with the aim of practicing alone and tosubsequently obtain feedback to the teacher.
This autonomous work will go with doubt resolution sessions, which can be face-to-face or non-face-to-face, scheduled at demand of students

Development plan

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Week	Description	Activity grup Teoria	Activity grup Pralab
1	Presentation + Unit 1 Introduction	Master class /Problem solving	Problem solving
2	Unit 2 Instruction Set	Master class / Problem solving	Lab Practical exercices
3	Unit 2 Instruction Set	Master class / Problem solving	Lab Practical exercices
4	Unit 2 Instruction Set	Master class / Problem solving	Problem solving
5	Unit 2 Instruction Set	Master class / Problem solving	Problem solving
6	Unit 3 Control Unit	Master class / Problem solving	Lab Practical exercices
7	Unit 3 Control Unit	Master class / Problem solving	PR1 exam
8	Unit 4 Memory	Master class / Problem solving	Problem solving
9	1st partial exam		
10	Unit 4 Memory	Master class / Problem solving	Problem solving
11	Unit 4 Memory	Master class / Problem solving	Lab Practical exercices
12	Unit 4 Memory	Master class / Problem solving	Problem solving
13	Unit 4 Memory	Master class / Problem solving	Lab Practical exercices
14	Unit 5 Input / Ouput	Master class / Problem solving	Problem solving
15	Unit 5 Input / Ouput	Master class / Problem solving	PR2 delivery
16, 17 and 18	2nd partial exam		
19	Seminars		
20	Recovery Exam		

Evaluation

Acr.	Evaluation activities	Weighting	Minimum mark	In group	Compulsatory	Recoverable
Mid-term 1 Block	Exam mid-term 1	30%	NO	NO	NO	YES
Mid-term 2 Block	Exam mid-term 2	40%	NO	NO	NO	YES
Practical Block	Practical lab exercises (PR1 + PR2)	15% + 15%	NO	PR1 NO / PR2 YES	NO	YES

The **assessment will be continuous** and is made up of three different assessment blocks with the following weights with respect to the final grade for the subject:

- Mid-term 1 block: 30%
- Mid-term 2 block: 40%
- Practical block: 30%

So, the final Mark for the subject will be:

Final Mark = Mid-term 1 block 30% + Mid-term 1 block partial exam+ Practical block 30%

All assessment activities are planned to be carried out face-to-face.

The mark of the Practical block of the previous course can be saved keeping the same mark obtained. If a student wishes to maintain it, they must explicitly request it from the teaching staff within the corresponding deadlines e published on the Virtual Campus of the subject.

The student who does not pass the continuous assessment with a mark equal to or greater than 5 will have the right to recover the Mid-term 1 and/or Mid-term 2 suspended block. It will be mandatory to recover any partial block with a mark lower than 4. The Practical block It can only be recovered if a student has a mark equal to or greater than 4 in both Mid-term blocks and has not passed the Practical block and has not passed the continuous assessment.

The student who has permission to be evaluated through the alternative evaluation (see requirements and procedure in the UdL evaluation regulations) will have to carry out the following evaluation activities:

- Final Exam corresponding to the subject associated with the Mid-term1 and Mid-term 2 block. This exam will weigh 70% of the

final grade.
- Practice 1, under the same conditions as a student who performs the continuous assessment.
- Practice 2, under the same conditions as a student who performs the continuous assessment.

The final grade for the alternative assessment will be calculated as:

Final mark of Alternative Assessment = 70% Final Exam + 15% Practice 1+15% Practice 2

The student who does not pass the alternative assessment with a grade equal to or greater than 5 will have the right to recover the Final Exam. If the student chooses to recover, it will be mandatory to recover the Final Exam if his mark was less than 4. The Practical block (Practice 1 and Practice 2) can only be recovered if the same conditions specified in the continuous evaluation.

Bibliography

BASIC BIBLIOGRAPHY
Organización y Arquitectura de Computadores. (7ª edición) Stallings W., Editorial Prentice Hall, 2006.
Computer Organization and Architecture (11th Edition) Stallings W., Editorial Pearson, 2019 (Versió actualitzada en anglès. No es comercialitza versió en català/castellà.)

Subject learning materials:
Francesc Giné. Apartat de Recursos de Sakai
Introducció al llenguatge assemblador. Simulador de Von Neumann.
Jordi Vilaplana, Albert Saiz, Eines 83, Edicions de la Universitat de Lleida, 2019

EXTENDED BIBLIOGRAPHY
Estructura y Diseño de Computadores. La interfaz hardware/Software.(4a edición)
Patterson D.A., Hennesy J.L, Edit. Reverte, 2011.
The Principles of Computer Hardware
Clements, A. Editorial OxfordUniversity Press.
Organización de computadores(5ª edición)
Hammacher C., Vranesic Z.,Zaky S., McGraw-Hill