DEGREE CURRICULUM

COMPUTER ORGANIZATION I

Coordination: ROVIRA MIQUEL, ALBERT

Academic year 2023-24

COMPUTER ORGANIZATION I 2023-24

Subject's general information

<table>
<tr><td>Subject name</td><td>COMPUTER ORGANIZATION I</td></tr>
<tr><td>Code</td><td>105002</td></tr>
<tr><td>Semester</td><td>1st Q(SEMESTER) CONTINUED EVALUATION</td></tr>
<tr><td>Typology</td><td>
<table>
<tr><th>Degree</th><th>Course</th><th>Character</th><th>Modality</th></tr>
<tr><td>Bachelor's Degree in Computer Engineering</td><td>1</td><td>COMMON/CORE</td><td>Attendance-based</td></tr>
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<tr><td>Course number of credits (ECTS)</td><td>6</td></tr>
<tr><td>Type of activity, credits, and groups</td><td>
<table>
<tr><th>Activity type</th><th>PRALAB</th><th>TEORIA</th></tr>
<tr><td>Number of credits</td><td>3</td><td>3</td></tr>
<tr><td>Number of groups</td><td>2</td><td>1</td></tr>
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<tr><td>Coordination</td><td>ROVIRA MIQUEL, ALBERT</td></tr>
<tr><td>Department</td><td>COMPUTER ENGINEERING AND DIGITAL DESIGN</td></tr>
<tr><td>Teaching load distribution between lectures and independent student work</td><td>Globally, the subject has 60 hours of face-to-face classes and 90 hours of independent student work.</td></tr>
<tr><td>Important information on data processing</td><td>Consult this link for more information.</td></tr>
<tr><td>Language</td><td>Catalan</td></tr>
<tr><td>Distribution of credits</td><td>3 credits Theory --> 30 hours of face-to-face classes + 45 hours of autonomous work from the student side.
3 credits Pralab (Problems + Lab) --> 30 hours of face-to-face classes + 45 hours of autonomous work from the student side.</td></tr>
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COMPUTER ORGANIZATION I 2023-24

Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
PUIGGROS FIGUERAS, DAVID	david.puiggros@udl.cat	6	
ROVIRA MIQUEL, ALBERT	albert.rovira@udl.cat	3	

Subject's extra information

Subject to be held during the first semester in the first course of the degree. It belongs to the main subject of Computer Organization inside the module of Basic Training.

To follow up the subject no previous knowledge of digital circuits is required. The knowledge adquired in the post-compulsory secondary education will be enough.

Learning objectives

- Learning the ways to represent information in a computer system and the mechanisms to manage this information.
- Studying the operation of the combinational and sequential modules and their function inside a computer
- Developing of the analysis and design processes of combinational and sequential circuits.
- Solving of circuits and ability of analysing several proposal.

Competences

Degree-specific competences

GII-FB5. Knowledge of the structure, organisation, operation and interconnection of the computer systems, the basics of programming, and its application to solve engineering problems.

GII-CR19. Ability to know, understand and evaluate computer structures and architecture, as well as the basic components which constitute them.

Degree-transversal competences

EPS1. Capacity to solve problems and prepare and defence arguments inside the area of studies.

EPS9. Capacity for unidisciplinary and multidisciplinary teamwork

Subject contents

A. THEORETICAL CONTENTS

1. Binary codification of the information

1.1. Binary codification

1.2. Numbering systems

1.3. Binary arithmetic

1.4. Signed number representation

1.5. Alphanumeric codes

2. Logic functions

2.1. Switching algebra

2.2. Logic gates

2.3. Logic functions

2.4. Minimization of logic functions

2.5. Incompletely specified functions

3. Combinational circuits

3.1. Two level gate structures

3.2. Analysis and design of combinational circuits.

3.3. Combinational systems.

3.3.1. Decoder

3.3.2. Encoder

3.3.3. Multiplexer

3.3.4. Demultiplexer

3.3.5. Comparator

4. Sequential circuits

4.1. Basic memory cell

4.2. Flip-flops

4.3. Direct set/reset inputs

4.4. Analysis aof sequential circuits

4.5. Design of sequential circuits

4.6. Basic sequential systems

4.6.1.Registers

4.6.2.Counters

B. PRACTICAL CONTENTS

Design of digital circuits using the ISIS PROTEUS simulator.

Practical activities:

- Design of a combinational circuit to carry out a specific function. (Theme 3)

- Design of a sequential circuit that passes for a predetermined sequence of states. (Theme 4)

Methodology

Classes are taught in face-to-face mode and are divided in different groups: theoretical group (Teo group) and problems/practices group (PraLab group).

The contents of the different kind of groups are divided in the following way:

Theoretical group: They are expositive lessons where they are shown the main contents on the subject.

PraLab group: they are classes to solve exercices and practices, related to the contents exposed in the Theoretical group, in a participative and interactive way.

Development plan

Week	Description	Activity grup Teoria	Activity grup Pralab

1	Binary codification of the information. Logic functions	Subject Introduction. Boolean Algebra.	Binary codification. Numeric Systems.
2	Binary codification of the information. Logic functions	Operators and logic gates	Binary Arithmetic.
3	Binary codification of the information. Logic functions	Representation of logic functions	Signed number representation. Alphanumeric codes
4	Logic functions	Minimization of logic functions	Exercises of logic functions
5	Logic functions	Incompletely specified functions	Exercises of logic functions
6	Combinational circuits	Two level gate structures	Exercises of logic functions
7	Combinational circuits	Analysis and design of combinational circuits	Exercises of combinational circuits
8	Combinational circuits	Basic combinational systems	Exercises of combinational circuits
9	1rst term Exam		
10	Combinational circuits	Basic combinational systems	Exercises of combinational circuits
11	Sequential circuits	Basic memory cell	Lab exercise of combinational circuits
12	Sequential circuits	Flip-flops	Exercises of sequential circuits
13	Sequential circuits	Analysis of sequential circuits	Exercises of sequential circuits
14	Sequential circuits	Design of sequential circuits	Exercicis circuits seqüencials
15	Sequential circuits	Basic sequential systems and modules	Lab exercise of sequential circuits
16 i 17	2nd term Exam		
18	Seminars		
19	Recovery Exam		

Evaluation

Acr.	Evaluation activities	Weighting	Minimum mark	In group	Compulsory	Recoverable
P1	1st term Exam	30%	NO	NO	NO	YES
P2	2nd term Exam	50%	NO	NO	NO	YES
PRA	Lab exercises	20%	NO	YES (if grup < = 2)	NO	NO

NOTA_FINAL = maximum (30% P1 + 50% P2, 80% P2) + 20% PRA
In order to pass the subject it is mandatory than **NOTA_FINAL is greater than or equal to 5**

In case of failling the subject, it is possible to do a recovery exam. The final mark will be calculated as explained next: N_rec: mark of the recovery exam. **NOTA_FINAL** = 80% N_rec + 20% PRA

Bibliography

· Lloris A., Prieto A., Parrilla L. Sistemas digitales. McGraW-Hill.
· Floyd T. Fundamentos de sistemas digitales. Prentice-Hall.
· Hammacher C., Vranesic Z., Zaky S. Organización de computadores (5ªedición). McGraw-Hill.
· Ercegovac M.D., Lang T. Digital Systems and Hardware/Firmware Algorithms. Jhon Wiley and Sons.
· Gascón M., Leal A., Peinado B. Problemas pràcticos de diseño lògico. Paraninfo