Universitat de Lleida

DEGREE CURRICULUM

DIGITAL ELECTRONICS

Coordination: ROIG MATEU, CONCEPCION

Academic year 2023-24

DIGITAL ELECTRONICS 2023-24

Subject's general information

Subject name	DIGITAL ELECTRONICS
Code	102120
Semester	1st Q(SEMESTER) CONTINUED EVALUATION
Typology	

Degree	Course	Character	Modality
Bachelor's Degree in Automation and Industrial Electronic Engineering	3	COMPULSORY	Attendance-based

Course number of credits (ECTS)	6
Type of activity, credits, and groups	

Activity type	PRALAB	PRAULA	TEORIA
Number of credits	0.4	2.6	3
Number of groups	4	2	1

Coordination	ROIG MATEU, CONCEPCION
Department	COMPUTER ENGINEERING AND DIGITAL DESIGN
Teaching load distribution between lectures and independent student work	60 hours of lecturer classes. 90 hours of indpendent student work.
Important information on data processing	Consult this link for more information.
Language	Catalan

DIGITAL ELECTRONICS 2023-24

Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
ROIG MATEU, CONCEPCION	concepcio.roig@udl.cat	3,8	
SOLA GIMENO, JOSEP MARIA	josepmaria.sola@udl.cat	6	

Learning objectives

Goals

- Learning basic digital devices.
- Establishing operation mechanisms of digital circuits.
- Understanding the applicability of digital circuits in de development of control circuitry and micropocessors.
- Proposing digital circuits able to solve specific problems, meeting constrains related to minimization and avalability of devices.
- Analysis of the behaviour of a specific digital circuit and deduction of the implemented logic functions .
- Given a specific situation to be solved with a digital circuit, find out the minimum circuit that responds for this solution.

Competences

Degree-specific competences

- GEEIA21. Knowledge of the basics and applications of digital electronics and microprocessors.
- GEEIA24. Capacity to design analog, digital and power electronic systems.

Degree-transversal competences

- EPS2. Capacity to gather and interpret relevant data, within the area of study, to judge and think about relevant subjects of social, scientific and ethical nature.
- EPS6. Capacity of analisys and synthesis.

Subject contents

A. Theory contents

Chapter 1. Logic functions

1.1. Switching algebra

1.2. Representation of functions.

1.3. Incompletely specified functions.

1.4. Simplification methods,

Chapter 2. Combinational circuits

2.1. Pulse and level signals.

2.2. Logic gates.

2.3. Positive and negative logic.

2.4. Two gate level circuits.

2.5. Analysis and design of combinational circuits.

2.6. Combinational systems.

Multiplexer/ Demultiplexer

Encoder/ Decoder

Comparators

One bit adder/ substractor

N bits adder

2.7. Programmable lógic devices

Chapter 3. Sequential circuits

3.1. Basic memory cell

3.2. Flip-flops

3.3. Synchronism

3.4. Analysis and design of synchronous sequential circuits

3.5. Registers and counters.

3.6. Analysis and design of assynchronous sequential circuits

B. Practices contents

1. Simulation of electronic digital circuits with the s/w PROTEUS (session 1)

2. Hardware implementation of digital circuits with components of 7400 family (session 2)

3. Hardware implementation of digital circuits with Fiels Programmable Gate Arrays (session 3)

4. Project design of a digital circuit using commercial combinational and sequential components using the s/w PROTEUS (sessions 4, 5, and 6 + brief)

Methodology

During the week, each student attends 2 hours in the Theory group and 2 hours in the problems/practices group (PraAula1 or PraAula2) .

- Classes of Theory group. Master classes devoted to presentation of new contents. (3 credits)

They are expositive classes where they are shown the main contents of the subject, supported by exercices and examples.

- Classes of problems/practices group (PraAula). Problem solving and practices. (3 credits)

Exercices related to the contents exposed in Theory classes are solved in a participative and interactive way. Also, laboratory practices of digital circuits are carried out using the simulator ISIS of Proteus, with FPGA and discrete components in the electronics laboratoy.

It is **COMPULSORY** that the students bring the following elements of individual protection (EPI) to the practices at the laboratory.

- Blue laboratory gown from UdL (unisex)
- Protection glasses
- Mechanical protection gloves

They can be purchased through the shop Údels of the UdL:

C/ Jaume II, 67 baixos
Centre the Cultures i Cooperació Transfronterera

http://www.publicacions.udl.cat/

Development plan

Week	Description	Activity Theory Group	Activity problems/practices group
1	Logic functions	Presentation of the subject. Switching algebra. Representation of functions.	Exercises of logic functions
2	Logic functions	Incompletely specified functions. Simplification methods	Exercises of logic functions
3	Combinational circuits	Pulse and level signals. Logic gates. Positive and negative logic. Two level circuits.	Exercises of combinational circuits
4	Combinational circuits	Analysis and design of combinational circuits.	Exercises of combinational circuits
5	Combinational circuits	Multiplexer/Demultiplexer. Encoder/Decoder.	Exercises of combinational circuits
6	Combinational circuits	Comparators. Adder/substractor of 1 bit	Practice 1

7	Combinational circuits	n bits adders	Practice 2
8	Combinational circuits	Programmable logic devices	Exercises of combinational circuits
9	Partial exams	Realization first partial exam	
10	Sequential circuits	Basic memory cell	Practice 3
11	Sequential circuits	Flip-flops and synchronism	Practice 4
12	Sequential circuits	Analysis and design of synchronous sequential circuits	
13	Sequential circuits	Analysis and design of synchronous sequential circuits	Practice 5
14	Sequential circuits	Registers and counters	Practice 6
15	Sequential circuits	Asynchronous circuits	Exercises of sequential circuits Project brief
16	Partial exams	Realization second partial exam	
17	Partial exams	Realization second partial exam	
18	Tutorials		
19	Recuperation exams	Exam recuperation, if necessary.	

Evaluation

The subject consists of the three following evaluation blocks:

N_P1: Mark of the combinational circuits block (first partial exam).

N_P2: Mark of the combinational and sequential circuits block (second partial exam)

N_Pr: Mark of the practices block, that consists of the following seven evaluation activities:

Six practices marks: N_PR1, N_PR2, N_PR3, N_PR4, N_PR5 and N_PR6 and the mark of the project report: N_Br.

The mark of the practices bloc is calculated as following:

N_Pr=10% N_Pr1 + 10% N_Pr2 + 10% N_Pr3 + 15% N_Pr4 + 15% N_Pr5 + 20% N_Pr6 + 20% N_Br

The final mark of the subject is calculated as following:
FINAL_MARK = maximum(20% N_P1 + 50% N_P2, 70% N_P2) + 30% N_Pr

To pass the subject it is necessary that FINAL_MARK is greater than or equal to 5.

In the case of not having passed the subject, there is the option to have a recuperation exam. In this case the FINAL_MARK is calculated as following:

N_rec: Mark of the recuperation exam.
FINAL_MARK = 70% N_rec + 30% N_Pr

ALTERNATIVE EVALUATION:

In the case of doing the alternative evaluation, a single exam will be carried out with a weight of **100%** of the grade, where all the contents of the subject, both theoretical and practical, will be assessed. The exam of the alternative evaluation will coincide with the 2on partial exam established in the exam schedule.

In the case of having a mark less than 5, and therefore not having passed the subject, a recuperation exam will be carried out, also with a weight of 100%, that will coincide with the date established for the recuperation exam of the subject in the exam schedule.

Bibliography

- Lloris A., Prieto A., Parrilla L. *Sistemas digitales*. McGraw-Hill.

- Gajski D. D. *Principios de Diseño Digital*. Prentice-Hall.

- García Zubía J. *Problemas resueltos de electrónica digital*. Thomson.

- Marcovitz A. *Introduction to logic design*. McGraw-Hill.

- Floyd T. L. Digital Fundamentals. Pearson