DEGREE CURRICULUM

DIGITAL ELECTRONICS

Coordination: ROIG MATEU, CONCEPCIÓN

Academic year 2019-20

DIGITAL ELECTRONICS 2019-20

Subject's general information

<table>
<tr><td>Subject name</td><td>DIGITAL ELECTRONICS</td></tr>
<tr><td>Code</td><td>102120</td></tr>
<tr><td>Semester</td><td>1st Q(SEMESTER) CONTINUED EVALUATION</td></tr>
<tr><td>Typology</td><td>
<table>
<tr><th>Degree</th><th>Course</th><th>Character</th><th>Modality</th></tr>
<tr><td>Bachelor's Degree in Automation and Industrial Electronic Engineering</td><td>3</td><td>COMPULSORY</td><td>Attendance-based</td></tr>
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<tr><td>Course number of credits (ECTS)</td><td>6</td></tr>
<tr><td>Type of activity, credits, and groups</td><td>
<table>
<tr><th>Activity type</th><th>PRALAB</th><th>PRAULA</th><th>TEORIA</th></tr>
<tr><td>Number of credits</td><td>0.4</td><td>2.6</td><td>3</td></tr>
<tr><td>Number of groups</td><td>4</td><td>2</td><td>1</td></tr>
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<tr><td>Coordination</td><td>ROIG MATEU, CONCEPCIÓN</td></tr>
<tr><td>Department</td><td>COMPUTER SCIENCE AND INDUSTRIAL ENGINEERING</td></tr>
<tr><td>Important information on data processing</td><td>Consult this link for more information.</td></tr>
<tr><td>Language</td><td>Catalan</td></tr>
<tr><td>Office and hour of attention</td><td>Concepció Roig: Friday from 13:00 h to 14:00 h,
Josep M. solà: Friday from 13:00 h to 14:00 h.</td></tr>
</table>

DIGITAL ELECTRONICS 2019-20

Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
ROIG MATEU, CONCEPCIÓN	concepcio.roig@udl.cat	3	
SAIZ VELA, ALBERT	albert.saiz@udl.cat	,8	
SOLA GIMENO, JOSEP MARIA	josepmaria.sola@udl.cat	6	

Learning objectives

Goals

- Learning basic digital devices.
- Establishing operation mechanisms of digital circuits.
- Understanding the applicability of digital circuits in de development of control circuitry and micropocessors.
- Proposing digital circuits able to solve specific problems, meeting constrains related to minimization and avalability of devices.
- Analysis of the behaviour of a specific digital circuit and deduction of the implemented logic functions .
- Given a specific situation to be solved with a digital circuit, find out the minimum circuit that responds for this solution.

Competences

Degree-specific competences

- GEEIA21. Knowledge of the basics and applications of digital electronics and microprocessors.
- GEEIA24. Capacity to design analog, digital and power electronic systems.

Degree-transversal competences

- EPS1. Ability to resolve problems and elaborate and defend arguments inside their field of study.
- EPS6. Capacity of analisys and synthesis.

Subject contents

Chapter 1. Logic functions

1.1. Switching algebra

1.2. Representation of functions.

1.3. Incompletely specified functions.

1.4. Simplification methods,

1.5. Multifuncional simplification.

Chapter 2. Combinational circuits

2.1. Pulse and level signals.

2.2. Logic gates.

2.3. Positive and negative logic.

2.4. Two gate level circuits.

2.5. Analysis and design of combinational circuits.

2.6. Combinational systems.

Multiplexer/ Demultiplexer

Encoder/ Decoder

Comparators

One bit adder/ substractor

N bits adder

Chapter 3. Sequential circuits

3.1. Basic memory cell

3.2. Flip-flops

3.3. Synchronism

3.4. Analysis and design of synchronous sequential circuits

3.5. Registers and counters.

3.6. Analysis and design of assynchronous sequential circuits

Chapter 4. Memories and programmable logic devices.

4.1. ROM Memory

4.2. Combinational PLD

4.3. Sequential PLD

Methodology

During the week, each student attends 2 hours of classes in Big Group and 2 hours in Medium Group.

- Classes of Big Group. **Master classes**. (3 credits)

They are expositive classes where they are shown the main contents of the subject, supported by exercices and examples.

- Classes of Medium Group. **Problem solving and practices**. (3 credits)

Exercices related to the contents exposed in Master classes are solved in a participative and interactive way. Also, laboratory practices of digital circuits are carried out using the simulator ISIS of Proteus. Besides, practices are carried out in the electronic laboratoy.

It is **COMPULSORY** that the students bring the following elements of individual protection (EPI) to the practices at the laboratory.

- Blue laboratory gown from UdL (unisex)
- Protection glasses
- Mechanical protection gloves

They can be purchased through the shop Údels of the UdL:

C/ Jaume II, 67 baixos

DIGITAL ELECTRONICS 2019-20

Centre the Cultures i Cooperació Transfronterera

http://www.publicacions.udl.cat/

Development plan

Week	Description	Activity Big Group	Activity Medium Group
1	Logic functions	Presentation of the subject. Switching algebra. Representation of functions.	Exercises of logic functions
2	Logic functions	Incompletely specified functions. Simplification methods	Exercises of logic functions
3	Combinational circuits	Pulse and level signals. Logic gates. Positive and negative logic. Two level circuits.	Exercises of combinational circuits
4	Combinational circuits	Analysis and design of combinational circuits.	Exercises of combinational circuits
5	Combinational circuits	Multiplexer/Demultiplexer. Encoder/Decoder.	Practice 1
6	Combinational circuits	Comparators. Adder/substractor of 1 bit	Exercises of combinational circuits
7	Combinational circuits	n bits adders	Practice 2
8	Sequential circuits	Basic memory cell	Exercises of sequential circuits
9	Partial exams	Realization first partial exam	
10	Sequential circuits	Flip-flops and synchronism	Exercises of sequential circuits
11	Sequential circuits	Analysis and design of synchronous sequential circuits	Practice 3
12	Sequential circuits	Registers and counters	Practice 4 (simulated part)
13	Sequential circuits	Analysis and design of assynchronous sequential circuits	Practice 5
14	Memories and programmable logic devices	ROM memory	Practice 4 (part implemented in the electronics lab.)
15	Memories and programmable logic devices.	Combinational and sequential PLD	Practice 4 (part implemented in the electronics lab.)
16	Partial exams	Realization second partial exam	
17	Partial exams	Realization second partial exam	
18	Tutorials		
19	Recuperation exams	Exam recuperation, if necessary.	

Evaluation

N_P1: Mark of first partial exam

N_P2: Mark of second partial exam.

N_Pr: Mark of practices.

The final mark of the subject is calculated as following:
FINAL_MARK = 20% N_P1 + 50% N_P2 + 30% N_Pr

To pass the subject it is necessary that FINAL_MARK is greater than or equal to 5.

In the case of not having passed the subject, there is the option to have a recuperation exam. In this case the FINAL_MARK is calculated as following:

N_rec: Mark of the recuperation exam.
FINAL_MARK = 70% N_rec + 30% N_Pr

Bibliography

- Lloris A., Prieto A., Parrilla L. *Sistemas digitales*. McGraw-Hill.

- Gajski D. D. *Principios de Diseño Digital*. Prentice-Hall.

- García Zubía J. *Problemas resueltos de electrónica digital*. Thomson.

- Marcovitz A. *Introduction to logic design*. McGraw-Hill.