DEGREE CURRICULUM

DIGITAL ELECTRONICS

Coordination: Concepció Roig Mateu

Academic year 2014-15

DIGITAL ELECTRONICS 2014-15

Subject's general information

Subject name	Digital Electronics
Code	102120
Semester	5
Typology	Compulsory
ECTS credits	6
Theoretical credits	3
Practical credits	3
Coordination	Concepció Roig Mateu
Office and hour of attention	Concepció Roig: Friday from 13:00 h to 14:00 h, Josep M. solà: Friday from 13:00 h to 14:00 h.
Department	Informàtica i Enginyeria Industrial
Modality	Presencial
Important information on data processing	Consult this link for more information.
Language	Català
Degree	Degree in Automation and Industrial Electronic Engineering
Office and hour of attention	Concepció Roig: Friday from 13:00 h to 14:00 h, Josep M. solà: Friday from 13:00 h to 14:00 h.
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DIGITAL ELECTRONICS 2014-15

Josep M. Solà
Concepció Roig Mateu

Learning objectives

Goals

- Learning basic digital devices.
- Establishing operation mechanisms of digital circuits.
- Understanding the applicability of digital circuits in de development of control circuitry and micropocessors.
- Proposing digital circuits able to solve specific problems, meeting constrains related to minimization and avalability of devices.
- Analysis of the behaviour of a specific digital circuit and deduction of the implemented logic functions .
- Given a specific situation to be solved with a digital circuit, find out the minimum circuit that responds for this solution.

Competences

Degree-specific competences

- GEEIA21. Knowledge of the basics and applications of digital electronics and microprocessors.
- GEEIA24. Capacity to design analog, digital and power electronic systems.

Degree-transversal competences

- EPS1. Ability to resolve problems and elaborate and defend arguments inside their field of study.
- EPS6. Capacity of analisys and synthesis.

Subject contents

Chapter 1. Binary codes

1.1. Number systems

1.2. Binary arithmetic.

1.3. Representation of signed number.

Chapter 2. Logic functions

2.1. Switching algebra

2.2. Canonical representation of functions.

2.3. Incompletely specified functions.

2.4. Simplification methods,

2.5. Multifuncional simplification.

Chapter 3. Combinational circuits

3.1. Pulse and level signals.

3.2. Logic gates.

3.3. Positive and negative logic.

3.4. Two gate level circuits.

3.5. Analysis and design of combinational circuits.

3.6. Combinational systems.

- Multiplexer/ Demultiplexer
- Encoder/ Decoder
- Comparators
- One bit adder/ substractor
- N bits adder

Chapter 4. Sequential circuits

4.1. Basic memory cell

4.2. Flip-flops

4.3. Synchronism

4.4. Analysis and design of sequential circuits

4.5. Design of synchronous sequential circuits.

4.6. Counters

4.7. Registers

Chapter 5. Memories and programmable logic devices.

5.1. ROM Memory

5.2. Combinational PLD

5.3. Sequential PLD

Evaluation

N_P1: Mark of first partial exam

N_P2: Mark of second partial exam.

N_Pr: Mark of practices.

The final mark of the subject is calculated as following:
FINAL_MARK = 20% N_P1 + 50% N_P2 + 30% N_Pr

To pass the subject it is necessary that FINAL_MARK is greater than or equal to 5.

In the case of not having passed the subject, there is the option to have a recuperation exam. In this case the FINAL_MARK is calculated as following:

N_rec: Mark of the recuperation exam.
FINAL_MARK = 70% N_rec + 30% N_Pr

Bibliography

- Lloris A., Prieto A., Parrilla L. *Sistemas digitales*. McGraw-Hill.

- Gajski D. D. *Principios de Diseño Digital*. Prentice-Hall.

- García Zubía J. *Problemas resueltos de electrónica digital*. Thomson.

- Marcovitz A. *Introduction to logic design*. McGraw-Hill.