DEGREE CURRICULUM

HARDWARE AND SOFTWARE VERIFICATION SYSTEMS

Academic year 2015-16

HARDWARE AND SOFTWARE VERIFICATION SYSTEMS 2015-16

Subject's general information

Subject name	HARDWARE AND SOFTWARE VERIFICATION SYSTEMS
Code	102044
Semester	2n Q Avaluació Continuada
Typology	Obligatòria
ECTS credits	6
Theoretical credits	3
Practical credits	3
Office and hour of attention	The meetings will be arranged with the professor on demand.
Department	Informàtica i Enginyeria Industrial
Modality	Presencial
Important information on data processing	Consult this link for more information.
Language	Spanish / English All the learning material, exercises and homework will be presented in English Classes can be given in English if students need so. Personal attention can also be given in English.
Degree	Degree in Computer Engineering
Distribution of credits	3 crèdits teoria 3 crèdits pràctica
Office and hour of attention	The meetings will be arranged with the professor on demand.
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HARDWARE AND SOFTWARE VERIFICATION SYSTEMS 2015-16

Ramón Béjar

Subject's extra information

To successfully address the subject, it is advisable to have previously taken courses with contents about:

- Computational Logic (that is present in many computer engineering university degrees).
- Artificial intelligence (that is present in many computer engineering university degrees).

So, students wanting to study this subject should have finished at least those computer engineering subjects.

Learning objectives

Expected learning outcomes linked to UdL strategic and cross-disciplinary competences :

- To know how to prepare technical documents with different presentation tools for digital documents (CT3).
- To know how to work with technical and scientific documents written in English (CT2).
- To understand the main problems encountered in the design of intelligent systems capable of reasoning and learning and knows how to analize the requirements in the design of these systems (EPS6)**.**

Expected learning outcomes linked to specific competences :

- To know and understand the fundamental problems of the formal specification of the behavior of programs (GII-C5).
- To know the formal specification of programs based on formal languages (GII-C5).
- To know how to use basic tools for semi-automatic verification of software, that need interaction with people to complete tasks that can not be automated 100%, and understand the limitations that the theoretical results on computability imposed on these tools (GII-C5 , GII-C6).

Competences

Strategic:

CT2. Mastering a foreign language, especially English.

CT3. Training Experience in the use of the new technologies and the information and communication technologies.

Cross-disciplinary:

EPS6. Capacity of analysis and synthesis.

Specific:

GII-C5 Capacity to acquire, obtain, formalise and represent the human knowledge in a computable form to solve problems by means of a computer system in any field of application, particularly in the ones related with computation, perception and performance in environments or intelligent surroundings.

GII-C6. Capacity to develop and evaluate interactive systems and of presentation of complex information and its application to solve problems of design of computer-person interaction.

Subject contents

1. Introduction to the verification of software and hardware

2. Formal verification of algorithms

3. Full Verification

    - Hoare Logic Calculus

    - Verification of While-Do programs

    - Partial versus full verification.

    - Forward verification with status updates

    - Verification of programs with the Key-Hoare tool

4. Partial Verification and Bug Finding

    - Verification systems through Bounded Model Checking (BMC)

    - Verification ANSI-C programs by CBMC tool

    - Hardware Verification by BMC

Methodology

There will be three types of activities:

1) Lectures (50% of the classes).

2) Classes for solving exercises, lab problems and mandatory assignments (50% of the classes).

3) Independent work outside class for finishing exercises and doing the mandatory assignments.

Development plan

The first part of the course will be devoted to complete verification of programs based on first-order logic techniques, and the second part to verification based on bounded model checking (BMC) and propositional logic.

Evaluation

The evaluation is carried out through the five following activities:

1. Exercises of formal verification of algorithms (20% of the mark)

2. Written test on full verification of programs with Hoare Logic (10% of the mark)

3. Practical exercise on full verification of programs with Hoare Logic with the tool Key-Hoare (30% of the mark)

4. Written test on partial verification programs BMC (10% of the mark)

5. Practical exercise on partial verification program with the BMC tool CBMC (30% of the mark)

Bibliography

All learning material will be provided during the course in the form of slides, lecture notes and manuals of the

different programs to be used. There is no convenient text book that can be used to follow the contents of this subject.