



DEGREE CURRICULUM  
**COMPUTER ARCHITECTURE**

Coordination: ROIG MATEU, CONCEPCIÓN

Academic year 2016-17

## Subject's general information

<b>Subject name</b>	COMPUTER ARCHITECTURE			
<b>Code</b>	102014			
<b>Semester</b>	2nd Q(SEMESTER) CONTINUED EVALUATION			
<b>Typology</b>	<b>Degree</b>	<b>Course</b>	<b>Typology</b>	<b>Modality</b>
	Double bachelor's degree: Degree in Computer Engineering and Degree in Business Administration and Management	2	COMPULSORY	Attendance-based
	Bachelor's Degree in Computer Engineering	2	COMPULSORY	Attendance-based
<b>ECTS credits</b>	6			
<b>Groups</b>	1GG,3GM			
<b>Theoretical credits</b>	3			
<b>Practical credits</b>	3			
<b>Coordination</b>	ROIG MATEU, CONCEPCIÓN			
<b>Department</b>	INFORMATICA I ENGINYERIA INDUSTRIAL			
<b>Teaching load distribution between lectures and independent student work</b>	Globally the subject has 60 hours of presential classes and 120 hours of individual working of students.			
<b>Important information on data processing</b>	Consult <a href="#">this link</a> for more information.			
<b>Language</b>	Catalan			
<b>Distribution of credits</b>	3 credits of big group (GG) for the theoretical part, 3 credits of medium group (GM) for problems/practices.			
<b>Office and hour of attention</b>	Monday and Thursday from 10 to 11 h. Room 3.13 EPS			

Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
ROIG MATEU, CONCEPCION	roig@diei.udl.cat	12	

## Subject's extra information

This subject is held during the second semester of the second course of the degree.

This is a compulsory subject.

To follow up the subject it is required to have the knowledge of functional units composing the computer system, that are studied in the previous subjects of Computer Organization I and II.

## Learning objectives

- Studying the global operation and the levels of the memory hierarchy in the computer.
- Learning the organization of the information in the memory system in order to have efficiency in the acces.
- Learning the pipeline mechanism to execute instructions inside the processor and evaluate its performance.
- Study the processes and the algorithms that are needed to carry out basic and complex arithmetic operations inside the arithmetic unit.
- Analyzing different solutions in terms of efficiency and cost. Being able to find which design solutions provide the best tradeoff between cost and performance.

## Competences

Degree-specific competences

- GII-FB5: Knowledge of the structure, organization, workings and inter-connexion of computer systems, the basis of their programming, and their applications in the resolution of engineering problems.
- GII-CRI9: Ability to know, understand and evaluate computer structures and architecture, as well as the basic components which constitute them.

Degree-transversal competences

- EPS5: Ability for abstraction and critical, logical and logical reasoning.

## Subject contents

### 1. Memory hierarchy

#### 1.1. Introduction

General concepts

Principle of locality

#### 1.2. *Cache memory*

Cache memory configurations

Mapping and identification of blocs

Bloc replacing algorithms

Writing policies

Data consistency

Cache performance

## 1.3. Main memory

Organization for improving performace

Alternative technologies

## 1.4. Virtual memory

Elements of virtual memory

Page table

TLB (Transaction Look-aside Buffer).

## 2. Pipeline processing

### 2.1. Basic concepts

### 2.2. Hazard management

Estructural hazards

Data hazards

Control hazards

### 2.3. Influcency of instruction set

### 2.4. Superescalar execution

## 3. Arithmetic processing

### 3.1. Adder circuits.

Half-adder, full-adder, parallel adder.

Carry-look-ahead.

adder/substractor circuit.

### 3.2. Binary multiplication algorithms.

### 3.3. Binary division algorithms

### 3.4. Floating point arithmetic

Floating point format

Approximate representation: rank and precision

Add and substract operations

Multiplication and division operations

## Methodology

Classes are divided in different groups, big group (GG), where they attend all the students of the subject and medium group (GM) where there only assist part of the students. The contents of the different kind of groups are divided in the following way:

GG: They are expositive classes where they are shown the main contents on the subject.

GM: they are classes to solve exercises related to the contents exposed in the GG classes, in a participative and interactive way. They also carry out lab practices of memory hierachy with the simulator SMPcaché and of pipeline execution with the simulator WinMIPS64.

## Development plan

Week	description	Activity GG	Activity GM
1	Memory hierarchy	Presentation of the subject. General concepts. Principle of locality.	Exercises of memory hierarchy
2	Memory hierarchy	Cache memory configurations. Mapping and identification of blocs	Exercises of memory hierarchy
3	Memory hierarchy	Bloc replacing algorithms. Writing policies	Exercises of memory hierarchy
4	Memory hierarchy	Data consistency	Exercises of memory hierarchy
5	Memory hierarchy	Cache performance	Practices of memory hierarchy
6	Memory hierarchy	Main memory. Virtual memory.	Practices of memory hierarchy
7	Pipeline processing	Basic concepts	Exercises of pipeline processing
8	Pipeline processing	Hazard management	Exercises of pipeline processing
9	Partial evaluation activities.	Realization of first partial exam	
10	Pipeline processing	Hazard management	Practices of pipeline processing
11	Pipeline processing	Influence of instruction set. Superscalar execution	Practices of pipeline processing
12	Arithmetic processing	Adder circuits	Exercises of arithmetic processing.
13	Arithmetic processing	Binary multiplication algorithms	Exercises of arithmetic processing.
14	Arithmetic processing	Binary division algorithms	Exercises of arithmetic processing.
15	Arithmetic processing	Floating point arithmetic	Exercises of arithmetic processing.
16 i 17	Partial evaluation activities	Realization of second partial exam	
18	Seminars		
19	Recuperation evaluation activities	Realization of the recuperation exam, if needed.	

## Evaluation

Acrr.	Evaluation activity	Weighing	Minimum mark	In group	Compulsory	Recoverable

P1	Exam 1 <sup>er</sup> Partial	30%	NO	NO	YES	YES
P2	Exam 2 <sup>on</sup> Partial	50%	NO	NO	YES	YES
PRA	Practices	20%	NO	YES (<=2)	YES	NO
<b>FINAL_MARK=30% P1+50% P2+20% PRA</b> To pass the subject, it is necessary that FINAL_MARK is greater than or equal to 5.						
In the case of not passing the subject there is the option of recuperating it separately for each of the two parts. In this case, the mark is calculated as following: N_rec_P1: recuperation mark of first partial exam N_rec_P2: recuperation mark of second partial exam <b>FINAL_MARK = 30% N_rec_P1 + 50% N_rec_P2 + 20% PRA</b>						

## Bibliography

Stallings W., *Organización y arquitectura de computadores*. (7 edición) Prentice-Hall.

Hamacher C., Vranesic Z., Zaky S. *Organización de computadores* (5ªedición). McGraw-Hill.

Ortega J., Anguita M., Prieto A. *Arquitectura de computadores*. Thomson.

Hennessy J. L., Patterson D. A. *Computer Architecture. A Quantitative Approach*. Morgan Kaufmann.