Universitat de Lleida

DEGREE CURRICULUM

COMPUTER ORGANIZATION II

Coordination: TOMAS CUÑAT, ROSA ANA

Academic year 2023-24

COMPUTER ORGANIZATION II 2023-24

Subject's general information

<table>
<tr><td>Subject name</td><td>COMPUTER ORGANIZATION II</td></tr>
<tr><td>Code</td><td>102003</td></tr>
<tr><td>Semester</td><td>2nd Q(SEMESTER) CONTINUED EVALUATION</td></tr>
<tr><td>Typology</td><td>
<table>
<tr><th>Degree</th><th>Course</th><th>Character</th><th>Modality</th></tr>
<tr><td>Bachelor's Degree in Computer Engineering</td><td>1</td><td>COMMON/CORE</td><td>Attendance-based</td></tr>
<tr><td>Double bachelor's degree: Degree in Computer Engineering and Degree in Business Administration and Management</td><td>1</td><td>COMMON/CORE</td><td>Attendance-based</td></tr>
<tr><td>Programa Acadèmic de Recorregut Successiu - Enginyeria Informàtica</td><td>1</td><td>COMMON/CORE</td><td>Attendance-based</td></tr>
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<tr><td>Course number of credits (ECTS)</td><td>6</td></tr>
<tr><td>Type of activity, credits, and groups</td><td>
<table>
<tr><th>Activity type</th><td>PRALAB</td><td>TEORIA</td></tr>
<tr><th>Number of credits</th><td>3</td><td>3</td></tr>
<tr><th>Number of groups</th><td>4</td><td>2</td></tr>
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<tr><td>Coordination</td><td>TOMAS CUÑAT, ROSA ANA</td></tr>
<tr><td>Department</td><td>COMPUTER ENGINEERING AND DIGITAL DESIGN</td></tr>
<tr><td>Teaching load distribution between lectures and independent student work</td><td>6 ECTS = 25x6 = 150 hours of load.
This load is distributed as following:
40% --> 60 hours of lectures.
60% --> 90 hours of independent student work.</td></tr>
<tr><td>Important information on data processing</td><td>Consult this link for more information.</td></tr>
<tr><td>Language</td><td>Catalan and/or Spanish</td></tr>
<tr><td>Distribution of credits</td><td>Josep Maria Flix 9
Rosanna Tomàs 6
Francesc Giné 3 (Supervisor)</td></tr>
</table>

COMPUTER ORGANIZATION II 2023-24

Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
ALMACELLAS ABELLANA, SERGI	sergi.almacellas@udl.cat	6	
FLIX ROVIRA, JOSE MARIA	josepmaria.flix@udl.cat	2,8	
GINE DE SOLA, FRANCESC	francesc.gine@udl.cat	0	
GUTIÉRREZ MARTOS, FERNANDO ELOY	fgutier6@xtec.cat	3,2	
TOMAS CUÑAT, ROSA ANA	rosana.tomas@udl.cat	6	

Subject's extra information

To follow this subject properly some previous knowledge/skills on computer organization are recommended. According to this, it must have taken the subject of Computer Organization I, which is scheduled in the first semester of the first course.

The skills acquired in this course are required to take the course of Computer Architecture of the second degree course.

Learning objectives

- Implement simple programs written in assembly language.
- Identify, differentiate and understand the operation of a computer, its components, as well as the basic structure of Von-Neumann.
- Know the phases of instruction execution.
- Be able to propose a basic structure for an instruction set.
- Identify the components of the control unit and their interaction.
- Be able to propose a basic structure for the main memory of a computer.
- Identify and understand the system input / output within the structure of a computer.
- Help other group members if necessary.
- Find and justify the best solution in a given time.

Competences

Degree-specific competences

- GII-FB3: Capacity to understand and master the basic concepts of discreet mathematics, logical, algorithmic and computational complexity, and its application to solve engineering problems.
- GII-FB4: Basic knowledge of the use and programming of computers, operating systems, databases and computer programs with applications in engineering.
- GII-FB5: Knowledge of the structure, organisation, operation and interconnection of the computer systems, the basics of programming, and its application to solve engineering problems.
- GII-CR17: Knowledge, design and efficient use of the types and data structure more suitable for solving a problem.
- GII-CR19: Capacity to know, comprise and evaluate the structure and architecture of computers, as well as the basic components that conform them.

Degree-transversal competences

- EPS1: Capacity to solve problems and prepare and defence arguments inside the area of studies.
- EPS5: Capacity of abstraction and of critical, logical and mathematical thinking.
- EPS9: Capacity for unidisciplinary and multidisciplinary teamwork.
- EPS12: To be motivated for the quality and steady improvement.

Subject contents

1.- Introduction

1.1. Structure of a Von-Neumann Computer

1.2. Interconnection Structures.

1.3. Instruction Cycle

2.- Instruction set

2.1. Introduction.

2.2. Formats of Instruction.

2.3. Addressing modes

2.4. Types of operations.

2.5. Von Neumann Simulator.

3. Control Unit

3.1. Introduction and Functions

3.2. Control Signals.

3.2. Hardwired Control Unit.

4. Memory Unit

4.1. Global Concepts

4.2. Memory Hierarchy.

4.3. Random Access Memory

5. Input/Output System

5.1. General I/O system.

5.2. Addressing I/O.

5.3. Control / synchronization of I/O: Check State and Interruptions.

5.4. Access to I/O Data: Program-Driven and Direct Memory Access.

Methodology

Large Group: theory class (3 ECTS)

- In this group, the theoretical contents of the subject, accompanied by illustrative examples, will be explained. As support material class, there are the slides of the subject, which can be downloaded from the CV Sakai.

Medium Group: Problems / Laboratory Classes (3 ECTS)

- In this group, solving problems from the collection will be alternated along with performing practices of assembly programming. The material of the Laboratory will be posted on the CV Sakai of the subject. The student must attend class practices with statements previously read.

Self study (distance learning)

- The student should independently solve problems not done in class, with the aim of practicing alone and to subsequently obtain feedback to the teacher.
- This autonomous work will go with doubt resolution sessions, which can be face-to-face or non-face-to-face, scheduled at demand of students.

Development plan

This scheduling is illustrative and it depends of the calendar of exams published by EPS. Any change in the scheduling will be published through the virtual campus of the subject.

COMPUTER ORGANIZATION II 2023-24

Week	Description	Large Group	Medium Group	Autonomous Work
1	Presentation + U1: Introduction	Presentation and U1	U1	Read Slides U1
2	U2: Instructions Set	Theory	Theory/Problems	Study Theory
3	U2: Instructions Set	Theory	Problems	Study Theory and Solve Problems
4	U2: Instructions Set	Theory	Problems	Study Theory and Solve Problems
5	U2: Instructions Set	Theory and Problems	Laboratory: Presentation of the Environment	Study Theory, Solve Problems and Read Practices
6	U3: Control Unit	Theory	Laboratory: Practice Assembler	Study Theory, Solve Problems and Read Practices
7	U3: Control Unit	Theory	Laboratory: Practice Assembler	Study Theory, Solve Problems and Read Practices
8	U3: Control Unit	Theory and Problems	Problems	Study Theory and Solve Exam Problems
9	Partial Exam 1			Study
10	U4: Memory	Theory	Exam 1 of Practices	Study Practice
11	U4: Memory	Theory	Problems	Study Theory and Solve Problems
12	U4: Memory	Theory	Problems	Study Theory and Solve Problems
13	U5: Input/Output	Theory	Laboratory: Practice 2 Input/Output	Study Theory, Solve Problems and develope Practice 2.
14	U5: Input/Output	Theory	Laboratory: Practice 2 Input/Output	Study Theory and Solve Problems and develope Practice 2.
15	U5: Input/Output	Problems	Submission of practice 2 Input/Output	Submission Practice 2 and Solve Exam Problems

16	Partial Exam 2	Exam		Study
17	Partial Exam	Exam		Study
18				
19	Retake Exam	Exam	Study	

Evaluation

The **assessment is continuous** and is made up of three different assessment blocks with the following weights with respect to the final grade for the subject:

- Mid-term 1 block: 30%
- Mid-term 2 block: 40%
- Practical block: 30%

Therefore, the final Mark for the subject will be:

Final Mark = Mid-term 1 block 30% + Mid-term 2 block partial exam+ Practical block 30%

Each block is made up of the assessment activities shown in the following Table.

Assessment Blocks	**Weight**	**Minimum Mark**	**Recovery**	**Assessment Activities**	**Weights**	**Individual**
Mid-term 1 Block	30%	NO	YES	Mid-term 1 Exam	30%	YES
Mid-term 2 Block	40%	NO	YES	Mid-term 2 Exam	40%	YES
Practical Block	30%	NO	YES	*Practice 1*	15%	YES
				Practice 2	15%	YES

All assessment activities are planned to be carried out face-to-face.

The mark of the Practical block of the previous course can be saved keeping the same mark obtained in that course. If a student wishes to maintain it, they must explicitly request it to he teaching staff within the corresponding deadlines published on the virtual vampus of the subject.

The student who does not pass the continuous assessment with a mark equal to or greater than 5 will have the right to recover the Mid-term 1 and/or Mid-term 2 suspended block. It will be mandatory to recover any partial block with a mark lower than 4. The Practical block can only be recovered if a student has a mark equal to or greater than 4 in both Mid-term blocks and has not passed the Practical block and has not passed the continuous assessment.

The student who has permission to be evaluated through the alternative evaluation (see requirements and procedure in the UdL evaluation regulations) will have to carry out the following evaluation activities:

- Final Exam corresponding to the subject associated with the Mid-term1 and Mid-term 2 block. This exam will weigh 70% of the final grade.
- Practice 1, under the same conditions as a student who performs the continuous assessment.
- Practice 2, under the same conditions as a student who performs the continuous assessment.

The final grade for the alternative assessment will be calculated as:

Final mark of Alternative Assessment = 70% Final Exam + 15% Practice 1+15% Practice 2

The student who does not pass the alternative assessment with a mark equal to or greater than 5 will have the right to recover the Final Exam. If the student chooses to recover, it will be mandatory to recover the Final Exam if his mark was less than 4. The Practical block (Practice 1 and Practice 2) can only be recovered with the same conditions specified in the continuous assessment.

Bibliography

Basical Bibliography

- *Organización y Arquitectura de Computadores.* (7ª edición)

  Stallings W., Editorial Prentice Hall, 2006.

- Computer Organization and Architecture (11th Edition)

  Satllings W,, Editorial Pearson, 2019 (English version and totally updatd of the 7th edition)

- *Apunts de l'Assignatura*.

  Francesc Giné. Apartat de Recursos de Sakai

- *Introducció al llenguatge assemblador. Simulador de Von Neumann.*

  Jordi Vilaplana, Albert Saiz, Eines 83, Edicions de la Universitat de Lleida, 2019.

Extended bibliography:

- *Estructura y Diseño de Computadores. La interfaz hardware/Software.* (4ª edición)

  Patterson D.A., Hennesy J.L, Edit. Reverte, 2011.

- *The Principles of Computer Hardware*

  Clements, A. Editorial OxfordUniversity Press.

- *Organización de computadores*(5ª edición)

  Hammacher C., Vranesic Z.,Zaky S., McGraw-Hill.