



Universitat de Lleida

DEGREE CURRICULUM
COMPUTER ORGANIZATION II

Coordination: GINE DE SOLA, FRANCESC

Academic year 2017-18

Subject's general information

Subject name	COMPUTER ORGANIZATION II			
Code	102003			
Semester	2nd Q(SEMESTER) CONTINUED EVALUATION			
Typology	Degree	Course	Typology	Modality
	Double bachelor's degree: Degree in Computer Engineering and Degree in Business Administration and Management	1	COMMON	Attendance-based
	Bachelor's Degree in Computer Engineering	1	COMMON	Attendance-based
ECTS credits	6			
Groups	1GG,4GM			
Theoretical credits	3			
Practical credits	3			
Coordination	GINE DE SOLA, FRANCESC			
Department	INFORMATICA I ENGINYERIA INDUSTRIAL			
Teaching load distribution between lectures and independent student work	<p>6 ECTS = 25x6 = 150 hours of load. This load is distributed as following: 40% --> 60 hours of lectures. 60% --> 90 hours of independent student work.</p>			
Important information on data processing	Consult this link for more information.			
Language	Catalan			
Distribution of credits	Albert Saiz: 9 Francesc Giné: 6			
Office and hour of attention	Francesc Giné: Thursday, from 16h to 17h in the 3.09 office of the EPS Albert Saiz: Wednesday, from 17h to 18h in the 1.06 office of the'EPS			

Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
GINE DE SOLA, FRANCESC	sisco@diei.udl.cat	6	Thursday from 17h to 19h in the office 3.09 of the EPS. It is needed a previous appointment.
SAIZ VELA, ALBERT	asaiz@diei.udl.cat	9	Friday from 13h to 14h in the office 1.06 of the EPS. It is needed a previous appointment.

Subject's extra information

To follow this subject properly some previous knowledge/skills on computer organization are recommended. According to this, it must have taken the subject of Computer Organization I, which is scheduled in the first semester of the first course.

The skills acquired in this course are required to take the course of Computer Architecture of the second degree course.

Learning objectives

- Implement simple programs written in assembly language.
- Identify, differentiate and understand the operation of a computer, its components, as well as the basic structure of Von-Neumann.
- Know the phases of instruction execution.
- Be able to propose a basic structure for an instruction set.
- Identify the components of the control unit and their interaction.
- Be able to propose a basic structure for the main memory of a computer.
- Identify and understand the system input / output within the structure of a computer.
- help other group members if necessary.
- Find and justify the best solution in a given time.

Competences

Degree-specific competences

- GII-FB3: Capacity to understand and master the basic concepts of discreet mathematics, logical, algorithmic and computational complexity, and its application to solve engineering problems.
- GII-FB4: Basic knowledge of the use and programming of computers, operating systems, databases and computer programs with applications in engineering.
- GII-FB5: Knowledge of the structure, organisation, operation and interconnection of the computer systems, the basics of programming, and its application to solve engineering problems.
- GII-CR17: Knowledge, design and efficient use of the types and data structure more suitable for solving a problem.
- GII-CR19: Capacity to know, comprise and evaluate the structure and architecture of computers, as well as the basic components that conform them.

Degree-transversal competences

- EPS1: Capacity to solve problems and prepare and defence arguments inside the area of studies.
- EPS5: Capacity of abstraction and of critical, logical and mathematical thinking.
- EPS9: Capacity for unidisciplinary and multidisciplinary teamwork.
- EPS12: To be motivated for the quality and steady improvement.

Subject contents

1.- Introduction

- 1.1. Structure of a Von-Neumann Computer
- 1.2. Interconnection Structures.
- 1.3. Instruction Cycle

2.- Instruction set

- 2.1. Introduction.
- 2.2. Formats of Instruction.
- 2.3. Addressing modes
- 2.4. Types of operations.
- 2.5. KIT Simulator.

3. Control Unit

- 3.1. CPU Structure and Functions
- 3.2. Hardwired Control Unit.
- 3.3. Microprogrammed Unit.

4. Memory Unit

- 4.1. Global Concepts
- 4.2. Memory Hierarchy.
- 4.3. Internal Memory

5. Input/Output System

- 5.1. General I/O system.
- 5.2. Addressing I/O.
- 5.3. Control / synchronization of I/O: Check State and Interruptions.
- 5.4. Access to I/O Data: Program-Driven and Direct Memory Access.

Methodology

Large Group: theory class (3 ECTS)

- In this group, the theoretical contents of the subject, accompanied by illustrative examples, will be explained. As support material class, there are the slides of the subject, which can be downloaded from the CV Sakai.

Medium Group: Problems / Laboratory Classes (3 ECTS)

- In this group, solving problems from the collection will be alternated along with performing practices of assembly programming. The material of the Laboratory will be posted on the CV Sakai of the subject. The student must attend class practices with statements previously read.

Self study (distance learning)

- The student should independently solve problems not done in class, with the aim of practicing alone and to subsequently obtain feedback to the teacher.

Development plan

Week	Description	Large Group	Medium Group	Autonomous Work
1	Presentation + U1: Introduction	Presentation and U1	U1	Read Slides U1
2	U2: Instructions Set	Theory	Theory	Study Theory
3	U2: Instructions Set	Theory	Problems	Study Theory and Solve Problems
4	U2: Instructions Set	Theory	Problems	Study Theory and Solve Problems

5	U2: Instructions Set	Theory and Problems	Laboratory: Presentation of the Environment	Study Theory, Solve Problems and Read Practices
6	U3: Control Unit	Theory	Laboratory: Practice 1	Study Theory, Solve Problems and Read Practices
7	U3: Control Unit	Theory	Laboratory: Practice 2	Study Theory, Solve Problems and Read Practices
8	U3: Control Unit	Theory and Problems	Problems	Study Theory and Solve Exam Problems
9	Partial Exam 1			Study
10	U4: Memory	Theory	Exam 1 of Practices	Study Practice
11	U4: Memory	Theory	Problems	Study Theory and Solve Problems
12	U4: Memory	Theory	Problems	Study Theory and Solve Problems
13	U5: Input/Output	Theory	Laboratory: Practice 4	Study Theory, Solve Problems and Read Practices
14	U5: Input/Output	Theory	Laboratory: Practice 5	Study Theory and Solve Problems
15	U5: Input/Output	Problems	Exam 2 of Practices	Study Practices and Solve Exam Problems
16	Partial Exam 2	Exam		Study
17	Partial Exam	Exam		Study
18				
19	Retake Exam	Exam	Study	

Evaluation

Acr.	Activities of Assessment	Weighting	Minimum Mark	Group	Mandatory	Recovery
E1	Partial Exam 1	30%	NO	NO	YES	YES
E2	Partial Exam 2	40%	NO	NO	YES	YES
P1	Practice 1	15%	NO	YES (<=2)	YES	YES
P2	Practice 2	15%	NO	YES (<=2)	YES	YES

Final Mark = 15% P1 + 15% P2 + 30% E1 + 40% E2

The evaluation will be continuous and consists of the following four tests with the following percentages of the final grade:

- First evaluable practice: 15%
- First partial exam: 30%
- Second evaluable practice: 15%
- Second partial exam: 40%

Therefore, the final grade for the course will be:

Final Mark = 15% First evaluable practice + 15% Second evaluable practice + 30% First partial examination + 40% Second partial exam.

The practices of the previous year are recognized on maintaining the same marks than in the previous year.

Those students who do not pass the continuous assessment with a score equal to or greater than 5 will be entitled to a retake exam, which will count 70% of the final mark or retake the practices. In this case, the final mark will be:

Final Mark = 15% First evaluable practice + 15% Second evaluable practice + 70% Retake exam (if the student chooses to retake the exam)

or

Final Mark = 30% Retake Exam of Practices + 30% First partial examination + 40% Second partial exam. (if the student chooses to retake the practice)

Bibliography

Basical Bibliography

- *Organización y Arquitectura de Computadores. (7ª edición)*
Stallings W., Editorial Prentice Hall, 2006.
- *Apunts de l'Assignatura.*
Francesc Giné. Apartat de Recursos de Sakai

Extended bibliography:

- *Estructura y Diseño de Computadores. La interfaz hardware/Software. (4ª edición)*
Patterson D.A., Hennesy J.L, Edit. Reverte, 2011.
- *The Principles of Computer Hardware*
Clements, A. Editorial Oxford University Press.
- *Organización de computadores (5ª edición)*
Hammacher C., Vranesic Z., Zaky S., McGraw-Hill.