DEGREE CURRICULUM

COMPUTER ORGANIZATION II

Coordination: Francesc Giné

Academic year 2014-15

COMPUTER ORGANIZATION II 2014-15

Subject's general information

Subject name	COMPUTER ORGANIZATION II
Code	102003
Semester	2nd Semester
Typology	Mandatory
ECTS credits	6
Groups	There is a main group, where the theory is explained, and 4 small groups, where the problems and practices are carried out.
Theoretical credits	0
Practical credits	0
Coordination	Francesc Giné
Office and hour of attention	Francesc Giné: Thursday, from 16h to 17h in the 3.09 office of the EPS Albert Saiz: Wednesday, from 17h to 18h in the 1.06 office of the'EPS
Department	Computer and Industrial Engineering
Modality	Presencial
Important information on data processing	Consult this link for more information.
Language	Catalan
Degree	Degree in Computer Engineering
Distribution of credits	Albert Saiz: 9 Francesc Giné: 6
Office and hour of attention	Francesc Giné: Thursday, from 16h to 17h in the 3.09 office of the EPS Albert Saiz: Wednesday, from 17h to 18h in the 1.06 office of the'EPS
E-mail addresses	asaiz@diei.udl.cat sisco@diei.udl.cat

COMPUTER ORGANIZATION II 2014-15

Albert Saiz
Francesc Giné de Sola

Subject's extra information

It mus have taken the subject of Computer Organization I, which is scheduled in the first semester.

Learning objectives

Associated with the competences of the degree:

- Implement simple programs written in assembly language.
- Meet the structure of an assembly simple program.
- Identify, differentiate and understand its operation, the components of a computer, as well as the basic structure of Von-Neumann.
- Know the phases of instruction execution.
- Be able to propose a basic structure for an instruction set.
- Know and understand the fields that make a instruction. As access data and how this information is encoded in an instruction.
- Identify the components of the control unit and their interaction.
- Understand and differentiate the wired and microprogrammed implementation of a control unit.
- Be able to define the behavior of the control unit.
- Know the memory hierarchy and understand how and where to act the main memory of a computer.
- Be able to propose a basic structure for the main memory of a computer.
- Identify and understand the system input / output within the structure of a computer.
- Differentiating components of peripheral input / output as well as its interaction with the CPU.
- Know the timing and mechanism of transfer of E / S.

Associated with generic skills:

- help other group members if necessary.
- Be able to justify the solution adopted.
- Find the best solution in a given time.
- Identify the knowledge base involved in solving the problem.

Competences

Degree-specific competences

- Capacity to understand and master the basic concepts of discreet mathematics, logical, algorithmic and computational complexity, and its application to solve engineering problems.
- Basic knowledge of the use and programming of computers, operating systems, databases and computer programs with applications in engineering.
- Knowledge of the structure, organisation, operation and interconnection of the computer systems, the basics of programming, and its application to solve engineering problems.
- Knowledge, design and efficient use of the types and data structure more suitable for solving a problem.
- Capacity to know, comprise and evaluate the structure and architecture of computers, as well as the basic components that conform them.

Degree-transversal competences

- Capacity to solve problems and prepare and defence arguments inside the area of studies.
- Capacity of abstraction and of critical, logical and mathematical thinking.
- Capacity for unidisciplinary and multidisciplinary teamwork.
- To be motivated for the quality and steady improvement.

Subject contents

1.- Introduction (4h F + 4h NF)

1.1. Structure of a Von-Neumann Computer

1.2. Interconnection Structures.

1.3. Instruction Cycle

2.- Instruction set (16h F + 28h NF)

2.1. Introduction.

2.2. Formats

2.3. Addressing modes

2.4. Types of operations.

2.5. KIT Simulator.

3. Control Unit (12h F + 24h NF)

3.1. CPU structure and Functions

3.2. Hardwired Control Unit.

3.3. Microprogrammed Unit.

4. Memory Unit (12h F + 20h NF)

4.1 Global Concepts

4.2 Memory hierarchy.

4.3 Internal Memory

5. Input/Output System (12h F + 24h NF)

5.1. General I/O system.

5.2.Addressing I/O.

5.3.- Control / synchronization I'E / S: Check state and interruptions.

5.4. Access to I/O Data: Program-Driven and Direct Memory Access.

P: Face-to-face NP:Non Face-to-cace

Methodology

Each week students will receive:

- Two hours of class in the main group, where the the theoretical contents are explained, accompanied by illustrative examples. As a support material of the class will follow the slides of the subject.
- Two hours of class in small groups, where we alternate resolving problems associated with the collection of theoretical explanations of the subject, along with practices.

The evaluation will be continuous and comprises four different tests:

- Two written tests.
- Two practical tests.

Development plan

- Week 1: Unit 1 Introduction.
- Week 2-5: Unit 2 Instructions Set
- Week 5-8: Unit 3 Control Unit
- Week 8: First Practice evaluable
- Week 9: First exam
- Week 10-12: Unit 4 Memory
- Week 12-15: Unit 5 E / S
- Week 15: Second practice evaluable
- Week 16-17: Second exam
- Week 19: Recovery exam.

Evaluation

The evaluation will be continuous and consists of the following four tests with the folowing percentages of the final grade:

- First evaluable practice: 15%
- First partial exam: 30%
- Second evaluable practice: 15%
- Second partial exam: 40%

Therefore, the final grade for the course will be:

Final Mark = 15% First evaluable practice + 15% Second evaluable practice + 30% First partial

examination + 40% Second partial exam.

The practices of the previous year are recognized on maintaining the same marks than in the previous year.

Those students who do not pass the continuous assessment with a score equal to or greater than 5 will be entitled to a recovery exam, which will count 70% of the final mark. In this case, the final mark will be:

Final Mark = 15% First evaluable practice+ 15% Second evaluable practice + 70% Recovery exam.

Bibliography

Basical Bibliography

- *Organización y Arquitecturade Computadores.* (7ª edición)

  Stallings W., EditorialPrentice Hall, 2006.

- *Apunts de l'Assignatura*.

  Francesc Giné. Apartat de Recursos de Sakai

Recommended bibliography:

- *Estructura y Diseño de Computadores. La interfaz hardware/Software.*(4ª edición)

  Patterson D.A., Hennesy J.L, Edit. Reverte, 2011.

- *The Principles of Computer Hardware*

  Clements, A. Editorial OxfordUniversity Press.

- *Organización de computadores*(5ª edición)

  Hammacher C., Vranesic Z.,Zaky S., McGraw-Hill.