DEGREE CURRICULUM

COMPUTER ORGANIZATION I

Coordination: ROIG MATEU, CONCEPCIÓN

Academic year 2016-17

COMPUTER ORGANIZATION I 2016-17

Subject's general information

Subject name	COMPUTER ORGANIZATION I
Code	102002
Semester	1st Q(SEMESTER) CONTINUED EVALUATION
Typology	<table><tr><th>Degree</th><th>Course</th><th>Typology</th><th>Modality</th></tr><tr><td>Double bachelor's degree: Degree in Computer Engineering and Degree in Business Administration and Management</td><td>1</td><td>COMMON</td><td>Attendance-based</td></tr><tr><td>Bachelor's Degree in Computer Engineering</td><td>1</td><td>COMMON</td><td>Attendance-based</td></tr></table>
ECTS credits	6
Groups	1GG,4GM
Theoretical credits	3
Practical credits	3
Coordination	ROIG MATEU, CONCEPCIÓN
Department	INFORMATICA I ENGINYERIA INDUSTRIAL
Teaching load distribution between lectures and independent student work	Globally, the subject has 60 hours of lecturer classes and 120 hours of independent student work.
Important information on data processing	Consult this link for more information.
Language	Catalan
Distribution of credits	Attending the partition in different groups, the number of credits of each proffesor is the following. Josep M. Solà 12 Concepció Roig Mateu 3
Office and hour of attention	Concepció Roig: Friday from 13:00 h. a 14:00 h. Josep M. Solà: Friday from 13:00 h. a 14:00 h.

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Teaching staff	E-mail addresses	Credits taught by teacher	Office and hour of attention
ROIG MATEU, CONCEPCION	roig@diei.udl.cat	3	
SOLA GIMENO, JOSEP MARIA	jmsola@diei.udl.cat	12	

Subject's extra information

Subject to be held during the first semester in the first course of the degree. It belongs to the main subject of Computer Organization inside the module of Basic Training.

To follow up the subject no previous knowledge of digital circuits is required. The knowledge adquired in the post-compulsory secondary eduaction will be enough.

Learning objectives

- Learning the ways to represent information in a computer system and the mechanisms to manage this information.
- Studying the operation of the combinational and sequential modules and their function inside a computer
- Developing of the analysis and design processes of combinational and sequential circuits.
- Solving of circuits and ability of analysing several proposal.

Competences

University of Lleida strategic competences

Degree-specific competences

GII-FB5. Knowledge of the structure, organisation, operation and interconnection of the computer systems, the basics of programming, and its application to solve engineering problems.

GII-CR19. Ability to know, understand and evaluate computer structures and architecture, as well as the basic components which constitute them.

Degree-transversal competences

- Ability to work in a unidisciplinary and multidisciplinary team
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EPS1. Capacity to solve problems and prepare and defence arguments inside the area of studies.

EPS9. Capacity for unidisciplinary and multidisciplinary teamwork.

Subject contents

1. Binary codification of the information

1.1. Binary codification

1.2. Number systems

1.3. Binary arithmetic

1.4. Signed number representation

1.5. Alphanumeric codes

2. Logic functions

2.1. Switching algebra

2.2. Logic gates

2.3. Logic functions

2.4. Minimization of logic functions

2.5. Incompletely specified functions

3. Combinational circuits

3.1. Two level gate structures

3.2. Analysis and design of combinational circuits.

3.3. Combinational systems.

3.3.1. Decoder

3.3.2. Encoder

3.3.3. Multiplexer

3.3.4. Demultiplexer

3.3.5. Comparator

4. Sequential circuits

4.1. Basic memory cell

4.2. Flip-flops

4.3. Direct set/reset

4.4. Analysis aof sequential circuits

4.5. Design of sequential circuits

4.6. Basic sequential systems

4.6.1.Registers

4.6.2.Counters

Methodology

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Classes are divided in different groups, big group (GG), where they attend all the students of the subject and medium group (GM) where there only assist part of the students. The contents of the different kind of groups are divided in the following way:

GG: They are expositive classes where they are shown the main contents on the subject.

GM: they are classes to solve exercices related to the contents exposed in the GG classes, in a participative and interactive way. they also carry out lab practices to solve digital circuits with the simulator ISIS of Proteus.

Practical activities:

- Design of a combinational circuit to carry out a specific function.

- Design of a sequential circuit that passes for a predetermined sequence of states..

Development plan

Week	Description	Activity GG	Activity GM
1	Binary codification of the information. Logic functions	Presentation of the subject. Switching algebra.	Binary codification. Number systems.
2	Binary codification of the information. Logic functions	Logic gates.	Binary arithmetic
3	Binary codification of the information. Logic functions	Representation of logic functions.	Signed number representation. Alphanumeric codes.
4	Logic functions	Minimization of logic functions.	Exercises of logic functions.
5	Logic functions	Incompletely specified functions	Exercises of logic functions.
6	Combinational circuits	Two level gate structures	Exercises of logic functions.
7	Combinational circuits	Analysis and design of combinational circuits.	Exercises of combinational circuits
8	Combinational circuits	Combinational systems.	Exercises of combinational circuits
9	Partial evaluation activities.	First partial exam	
10	Combinational circuits	Combinational systems.	Exercises of combinational circuits
11	Sequential circuits	Basic memory cell	Practice of combinational circuits
12	Sequential circuits	Flip-flops	Exercises of sequential circuits.
13	Sequential circuits	Analysis of sequential circuits	Exercises of sequential circuits.
14	Sequential circuits	Design of sequential circuits	Exercises of sequential circuits.
15	Sequential circuits	Basic sequential systems	Practice of sequential circuits.
16 i 17	Partial evaluation activities.	Second partial exam	
18	Seminars		
19	Recuperation evaluation activities.	Recuperation exam, if needed.	

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Evaluation

Acr.	Evaluation activity	Weighing	Minimum mark	In group	Compulsory	Recoverable

P1	*Exam 1er Partial*	30%	NO	NO	YES	YES
P2	*Exam 2on Partial*	50%	NO	NO	YES	YES
PRA	*Practices*	20%	NO	YES (<=2)	YES	NO

FINAL_MARK = maximum(30% P1 + 50% P2, 80% P2) + 20% PRA
To pass the subject it is necessary that FINAL_MARK is greater than or equal to 5.

In the case of not passing the subject, there is the option to do a recuperation exam. In this case the FINAL_MARK is calculated as:
N_rec: mark of the recuperation exam
FINAL_MARK = 80% N_rec + 20% N_Pr

Bibliography

· Lloris A., Prieto A., Parrilla L. *Sistemas digitales*. McGraW-Hill.

· Floyd T. *Fundamentos de sistemas digitales*. Prentice-Hall.

· Hammacher C., Vranesic Z., Zaky S. *Organización de computadores* (5ªedición). McGraw-Hill.

· Ercegovac M.D., Lang T. *Digital Systems and Hardware/Firmware Algorithms*. Jhon Wiley and Sons.

· Gascón M., Leal A., Peinado B. *Problemas pràcticos de diseño lògico*. Paraninfo.