Universitat de Lleida

DEGREE CURRICULUM

ESTRUCTURA DE COMPUTADORES I

Academic year 2013-14

COMPUTER ORGANIZATION I 2013-14

Subject's general information

Subject name	ESTRUCTURA DE COMPUTADORES I
Code	102002
Semester	1r Q Avaluació Continuada
Typology	Troncal
ECTS credits	6
Theoretical credits	0
Practical credits	0
Department	Informàtica i Enginyeria Industrial
Important information on data processing	Consult this link for more information.
Language	Catalan
Distribution of credits	Josep M. Solà 4.8 Concepció Roig Mateu 6
Office and hour of attention	Concepció Roig: divendres de 13:00 h. a 14:00 h.

COMPUTER ORGANIZATION I 2013-14

Josep M. Solà
Concepció Roig Mateu

Subject's extra information

The course as part of the academic plan

Subject to be held during the first semester in the first course of the degree. It belongs to the main subject of Computer Organization inside the module of Basic Training.

Learning objectives

See competences

Competences

University of Lleida strategic competences

Degree-specific competences

- Knowledge of the structure, organization, workings and inter-connexion of computer systems, the basis of their programming, and their applications in the resolution of engineering problems.

Goals

  - Learning the ways to represent information in a computer system and the mechanisms to manage this information.

- Ability to know, understand and evaluate computer structures and architecture, as well as the basic components which constitute them.

Goals

  - Studying the operation of the combinational and sequential modules and their function inside a computer.

Degree-transversal competences

- Ability to resolve problems and elaborate and defend arguments inside their field of study.

Goals

  - Developing of the analysis and design processes of combinational and sequential circuits.

- Ability to work in a unidisciplinary and multidisciplinary team.

Goals

  - Solving of circuits in a collabortive way and ability of analysing several proposal.

Subject contents

1. Binary codification of the information

1.1. Binary codification

1.2. Number systems

1.3. Binary arithmetic

1.4. Signed number representation

1.5. Alphanumeric codes

2. Logic functions

2.1. Switching algebra

2.2. Logic gates

2.3. Logic functions

2.4. Minimization of logic functions

2.5. Incompletely specified functions

3. Combinational circuits

3.1. Two level gate structures

3.2. Analysis and design of combinational circuits.

3.3. Combinational systems.

3.3.1. Decoder

3.3.2. Encoder

3.3.3. Multiplexer

3.3.4. Demultiplexer

3.3.5. Comparator

4. Sequential circuits

4.1. Basic memory cell

4.2. Flip-flops

4.3. Direct set/reset

4.4. Analysis aof sequential circuits

4.5. Design of sequential circuits

4.6. Basic sequential systems

4.6.1.Registers

4.6.2.Counters

5. Arithmetic circuits

5.1. Half-adder

5.2. Full-adder

5.3. N bits parallel adder

5.4. Carry-look ahead

Evaluation

N_P1: nota examen primer parcial.

N_P2: nota examen segon parcial.

N_Pr: nota de pràctiques

La nota de l'assignatura es calcula aplicant els següents percentatges:

NOTA_FINAL = 30% N_P1 + 50% N_P2 + 20% N_Pr

Per tenir superada l'assignatura cal que NOTA_FINAL sigui major o igual que 5.

En cas de no haver superat l'assignatura, es pot anar a l'examen de recuperació. En aquest cas la nota es calcularà de la següent manera:

N_rec: nota de l'examen de recuperació.

NOTA_FINAL = 80% N_rec + 20% N_Pr

Bibliography

· Lloris A., Prieto A., Parrilla L. *Sistemas digitales*. McGraW-Hill.

· Floyd T. *Fundamentos de sistemas digitales*. Prentice-Hall.

· Hammacher C., Vranesic Z., Zaky S. *Organización de computadores* (5ªedición). McGraw-Hill.

· Ercegovac M.D., Lang T. *Digital Systems and Hardware/Firmware Algorithms*. Jhon Wiley and Sons.

· Gascón M., Leal A., Peinado B. *Problemas pràcticos de diseño lògico*. Paraninfo.